REMARKS

The Examiner is thanked for the thorough examination of the present application the allowance of claims 16-17, 19, 20, and 22-25, and the indication that 6-8, 10-11, 14, 18, 21, and 26 embody allowable subject matter. The Office Action, however, tentatively rejected the remaining claims 1-15, 18, and 21. In response to the Office Action, Applicant submits the foregoing amendments and the following remarks.

Allowable Subject Matter and Claim Amendments

The Office Action stated that claims 6-8, 10-11 and 14 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112 and to include all of the limitations of the base claim and any intervening claims. Similarly, the Office Action stated that claims 18, 21 and 26 would be allowable if rewritten to overcome the rejections under 35 U.S.C. 112.

Claim 1 has been amended to recite forming deposits of said first layer of dielectric on the top surface of the interconnect lines. Support for this limitation can be found in Fig. 5 of the specification. Accordingly, the amendment adds no new matter to the application.

Claims 3, 6, 8, 10-11, 14-15, 18 and 26 have been amended to provide antecedent support for certain features, to thereby overcome the rejections under 35 U.S.C. 112, second paragraph. Claims 7 and 21 are cancelled.

Reconsideration of the application, as amended, is respectfully requested.

Objection to the Specification

The Office Action objected to the specification for failing to provided proper antecedent support for subject matter in claims 7 and 21. Applicant has cancelled these claims, thereby rendering this objection moot.

Claim Rejections- 35 USC 112

The Office Action rejected claims 3, 7-8, 10, 11, 14, 15, 18, 21 and 26 under 35 U.S.C. § 112, second paragraph for various noted reasons of indefiniteness. Again, claims 7 and 21 are cancelled, thereby rendering the rejections of these claims moot. Claims 3, 8, 10, 11, 14, 15, 18, and 26 have been amended to address and overcome the rejections of those claims.

Specifically, in claims 3 and 18, the limitation "the SAC process" has been amended to "a SAC process." Claims 8, 10, and 11 have been amended to now depend from claim 6, which provides antecedent support for the limitations "said exposed top corners" and "the partially exposed top corners" of claims 8, 10 and 11. Claim 14 has been amended to depend from claim 12, which include the antecedent basis for the limitation "said spacer" of claim 14. Claim 15 has been amended to depend from claim 14, which provides antecedent support for the limitation "said deposited of PE-oxide or PE-TEOS" of claim 15. Also, the limitation "said conducting line pattern" of claim 15 has been amended to "said pattern of interconnect lines". The antecedent basis for the limitation of "said pattern of interconnect lines" can be found in independent claim 1, and claim 15 depends from independent claim 1. Therefore, there are sufficient antecedent bases for these limitations of claim 15. Finally, in claim 26, the limitation of "said conducting line pattern" has been

amended to "said pattern of interconnect lines". The antecedent basis for the limitation "said pattern of interconnect lines" can be found in independent claim 16, and claim 26 depends from independent claim 16.

For at least the foregoing reasons, Applicant submits that all rejections under 35 U.S.C. § 112, second paragraph have been properly addressed and should be withdrawn.

Claim Rejections- 35 USC 103

Claims 1-4, 12 and 15 stand rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Hsueh et al. (US 5,990,009) in view of Lee (US 5,663,092). Applicant respectfully requests reconsideration and withdrawal of this rejection.

As amended herein, independent claim 1 recites:

> 1. A method of filling gaps between a pattern of interconnect lines forming a wiring structure on a semiconductor substrate, said interconnect lines having a top surface further having sidewalls, comprising the steps of:
>
> providing a semiconductor substrate said substrate having a surface;
>
> creating a network of interconnect lines on said surface of said substrate whereby said interconnect lines are separated by holes having bottoms between said interconnect lines thereby leaving said surface of said substrate partially exposed over said bottoms of said holes between said interconnect lines;
>
> depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate;
>
> ***performing an etch back of said first layer of dielectric thereby forming deposits of said first layer of dielectric on the top surface of the interconnect lines***;
>
> depositing a second layer of dielectric having a surface over said etched back first layer of dielectric;
>
> etching said second layer of dielectric thereby creating exposed portions of said first layer of dielectric; and

depositing a layer of oxide over said etched second layer of dielectric thereby including said exposed portions of said first layer of dielectric.

(*Emphasis added*). Claim 1 patently defines over the cited art for at least the reasons that the cited art fails to disclose the features emphasized above.

As reflected above, independent claim 1 clearly defines depositing a first layer of dielectric having a surface over said interconnect lines wiring structure thereby including said exposed surface of said semiconductor substrate and performing an etch back of said first layer of dielectric thereby forming deposits of said first layer of dielectric on the top surface of the interconnect lines.

As disclosed in Figs. 4-5 of the present application, the first layer of dielectric 40 covers the interconnect lines 20 and the exposed surface of the semiconductor substrate 10. Then, the first layer of dielectric 40 is etched back to form deposits of the first layer of dielectric 52 on the top surface of the interconnect lines 20.

In contrast, as disclosed in Fig. 5J of Hsueh, the first insulating layer 114, covering the interconnect layers 110 and the exposed surface of the insulating layer 102, is etched to remove the deposits of the first insulating layer 114 over the interconnect layer 110. Even though insulating layers 112 remain on the top surfaces of the interconnect layers 110, the insulating layers 112 do not cover the exposed surface of the insulating layer 102. Thus, the insulating layers 112 cannot be properly equated to the claimed first layer of dielectric.

As disclosed in Fig. 6 of Lee, after etching process, the insulating layer 120 is only on the sidewalls of the capped gate lines 112. The insulating layers 120 do not remain on the top surface of the capped gate lines 112. Even though insulating regions 117 remain

on the top surfaces of the gate lines 114, the insulating regions 117 do not cover the exposed surface of the substrate 100. Thus, the insulating regions 117 cannot be properly equated to the claimed the first layer of dielectric.

Accordingly, even if properly combined, Hsueh and Lee (collectively) fail to teach or suggest the limitation of "forming deposits of said first layer of dielectric on the top surface of the interconnect lines," as expressly recited in claim 1. For at least this reason, the rejection of claim 1 should be withdrawn.

Claims 2-5, 9, 12-13, and 15 depend from independent claim 1 and therefore define over the cited art for at least the same reasons. *In re Fine*, 837 F.2d 1071, 5 U.S.P.Q.2d 1596, 1600 (Fed. Cir. 1988).

CONCLUSION

In view of the foregoing, it is believed that all pending claims are in proper condition for allowance. If the Examiner believes that a telephone conference would expedite the examination of the above-identified patent application, the Examiner is invited to call the undersigned.

A credit card authorization is provided herewith to cover the fee associated with the accompanying petition for extension of time. No additional fee is believed to be due in connection with this submission. If, however, any additional fee is deemed to be payable, you are hereby authorized to charge any such fee to Deposit Account No. 20-0778.

Respectfully submitted,

/Daniel R. McClure/

By: _____

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